Inverted Process Implementation of Monolithic Graphene Mixer

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Abstract

A monolithic graphene-based passive resistive FET mixer is implemented by a novel inverted process, which incorporates two routing layers and is implemented on 8" wafers. The process is CMOS compatible with passive elements monolithically integrated. The mixer functionality is demonstrated at f_{RF}=5.1GHz and f_{LO}=5GHz. It features a conversion loss of -32dB at a fixed LO power P_{LO}=0dBm.

Researchers have used individual graphene field-effect transistors (GFETs) connected to external passive components to realize graphene circuits. Graphene monolithic integrated circuits, on the other hand, could greatly expand graphene technological impacts. Pioneer researchers have made such attempts. Lin et al. has demonstrated graphene circuits integrated on a single SiC wafer which opened up the graphene integration possibility [1]. Han et al. moved forward by utilizing CVD graphene and fabricated GHz-range graphene ICs in IBM 200 mm silicon fab [2].

Unlike conventional ICs in which field-effect transistors are formed on Si wafers with upper layers of interconnect, this work proposes a novel inverted graphene integration approach. CMOS compatible two-layer-routing technology on 8'' wafer is utilized to form pre-patterned IC structures which include inductors, interconnects, pads and buried GFET gate/source/drain regions. Afterwards, large-scale monolayer graphene synthesized by CVD methods is transferred onto the pre-patterned dies to form graphene ICs.

A $1\mu m$ thick SiO_2 layer was first thermally grown on the 8-inch Si substrate, as shown in Fig. 1. Passive components, four-turn inductors in this case, were formed in the first metal layer (500nm thick Al) together with necessary interconnects. After interlayer passivation ($1\mu m$ SiO_2), the second metal layer (500nm thick Al) was utilized to define GFET gate/source/drain regions, which enabled an additional layer of interconnects. Chemical-Mechanical Polishing (CMP) was introduced to ensure the planarization of the fabricated wafer. The GFET employs a two-finger structure with W/L dimension of $19\mu m/0.5\mu m$. 3.8 nm thick HfO_2 (EOT 1nm) was deposited to form the gate dielectric by atomic layer deposition (ALD) method. Buried source/drain regions were exposed, which formed graphene source/drain contacts in the following steps.

Graphene was transferred to patterned dies and was defined by photolithography and O_2 plasma etching. Then, 40nm Pt was sputtered to form Al-graphene-Pt sandwich structure source/drain contacts [3]. Fig. 2 shows the optical microcopy image of an as-fabricated graphene frequency multiplier circuit, with the inset showing a GFET in the IC. The entire IC including pads is about $1mm^2$.

DC characteristics of the fabricated $19\mu m \times 2$ wide GFET with gate length of 500nm are shown in Fig. 3. Peak transconductance reaches $21\mu S/\mu m$ under 0.1V V_{ds} bias, as shown in Fig 3(a). I_{ds}-V_{ds} curves are shown in Fig. 3(b), with the peak current density of $400\mu A/\mu m$. Fig. 4 shows the RF characteristics of the GFET from s-parameter measurements. Careful de-embedding procedures have been performed. Current gain (h_{21}) and maximum unilateral gain decreases with increasing frequency at a rate close to $-20dB/dec$. f_T equals 17GHz and f_{max} reaches 15.2GHz. The f_{max}/f_T ratio is as high as 0.89.

For RF up- or down- conversion linear mixers, passive resistive FET mixers have been preferred [4]. 500nm-gate-length GFET is employed to form a graphene-based passive resistive FET mixer, with the schematic shown in Fig. 5(a). Two high-frequency signals, an RF signal at a frequency f_{RF} and a local oscillator (LO) signal at a frequency f_{LO}, are applied to the drain and the gate of the GFET, respectively. With no drain bias applied, no dc power dissipation is consumed. With an input RF power of 0dBm at 5.1GHz and LO power of 0dBm at 5GHz, the IF power at 100MHz results in -32dBm, as shown in Fig. 5(b).

In summary, a GFET resistive mixer formed by a novel inverted process and with good performance is implemented. Passive elements and interconnects are integrated monolithically. The graphene technology is CMOS compatible and offers further potential to be integrated with silicon electronics.

References

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[2] S. J. Han, et al, IEDM (2011) pp. 2.2.1-2.2.4.

[3] A. D. Franklin, et al, IEEE Electron Device Letters, 1(2012) pp. 17-19.
[4] J. S. Moon, et al, IEEE Electron Device Letters, 3(2013) pp. 465-467.

Figures

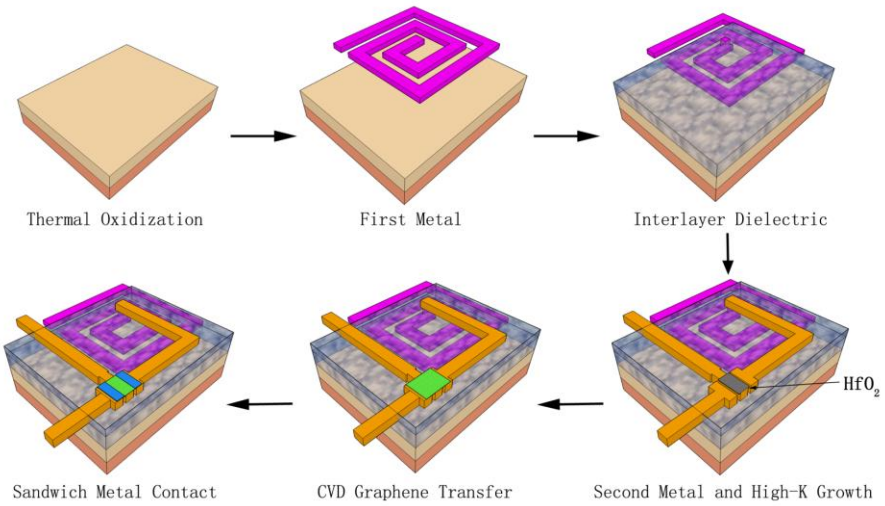

Fig. 1. Inverted process flow.

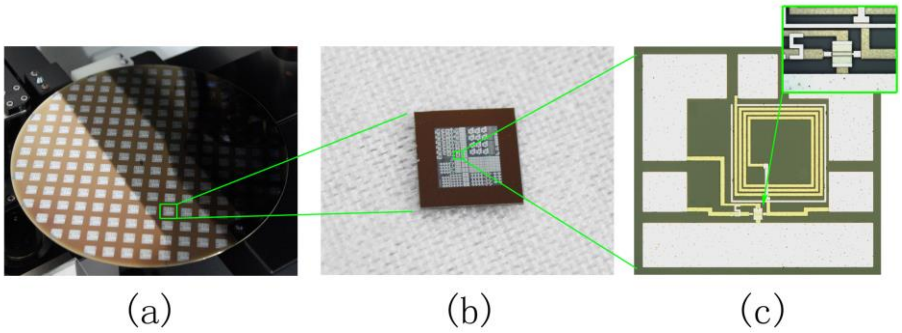

Fig. 2. Photographs of (a) an 8" graphene IC wafer and (b) single patterned die. (c) Optical microscope image of a fully-processed GFET resistive mixer with inset of the GFET in the IC.

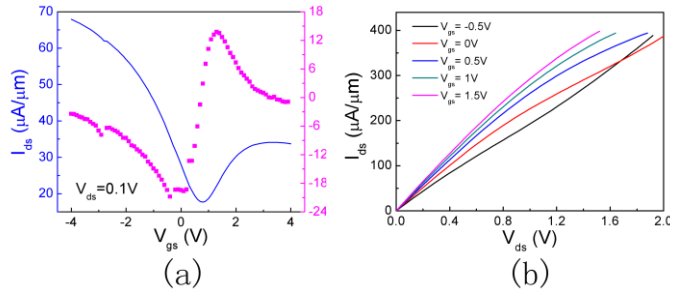

Fig. 3. (a) Transfer curve and transconductance of a 500nm-gate-length GFET at V_{ds} = 0.1V. (b) Output characteristics of the device.

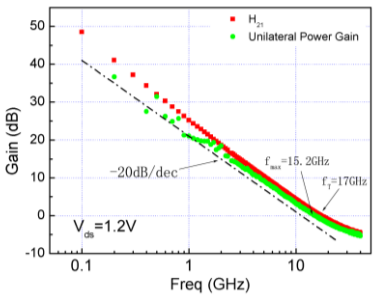

Fig. 4. f_{max} and f_T result in 15.2GHz and 17GHz, respectively.

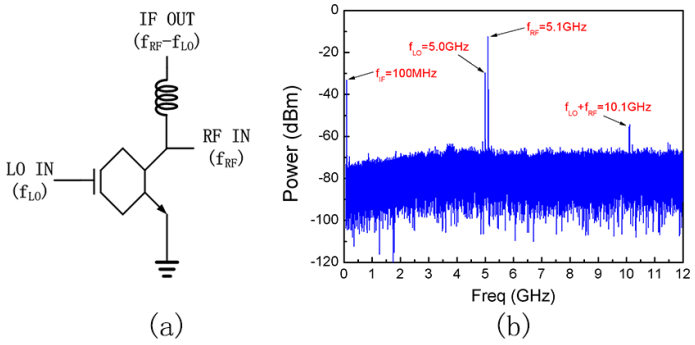

Fig. 5. (a) Schematic of the proposed GFET resistive mixer. (b) Output spectrum, between 0 and 12 GHz, of the mixer taken from the spectrum analyzer with f_{RF}=5.1GHz and f_{LO}=5GHz.